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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/702,593	10/31/2000	Cary A. Coutant	10001275-1	1046

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EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2122	4

DATE MAILED: 04/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/702,593	COUTANT ET AL.	
	Examiner	Art Unit	
	Chuck O Kendall	2122	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed 1/27/04.

2. Claims 1 – 16 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al. USPN 5,276,881 (hereinafter Chan).

Regarding claims 1 & 16, Chan anticipates a computer-implemented method, and a computer program (60:60 – 65) for switching between multiple implementations of a routine in a library of routines that are linked with an application program that is hosted by a computer system, comprising:

compiling a plurality of implementations of a routine into respective object code modules, the routine having an associated name and each implementation adapted to a selected hardware configuration (60: 13 – 17 see 1338, and mapping register set also refer to ,60:30 – 35);

associating the object code modules with the name of the routine and respective sets of hardware characteristics (60:33 – 40, see mapping register set to target computer platform); and

resolving when the application program is loaded into memory of the computer system, a reference to the routine using the sets of hardware characteristics and a hardware configuration of the system (55:60 – 65).

Regarding claim 2, the method of claim 1, further comprising establishing a symbol table having a plurality of entries, each entry including a name of a routine and a reference to an object code module in the library (FIG.13, 1306,1308, 1310 & 1312 also see associated text 58: 44 – 53, " The low level Generator 1322, uses the Symbol Table 1312 and the Type Table 1306 to bind data objects to the target computer...").

Regarding claim 3, the method of claim 2, further comprising, for the routine having a plurality of implementations, adding a plurality of entries to the symbol table and associating respective sets of hardware characteristics with the plurality of entries (48:1 – 15, for adding entries see " ...creates a Symbol Table 1134 and a Type Table 1138." also see 58: 44 – 53, as previously noted above in claim 2).

Regarding claim 4, the method of claim 3, wherein the hardware characteristics include at least one of clock speed of the processor, processor model, cache configuration of the system, hardware operation latency times (60:35 – 40, see file management information (configuration), (note Applicant claims " atleast one of...")), instruction set characteristics, bypass characteristics, branch prediction behavior, pre-fetching capability, information describing stall conditions, branch penalties, size and associativity of processor data structures (58:10 – 28, see configuration file, and register file sizes), queue sizes for out-of-order or decoupled processors, and the number of processors in a multiprocessor system.

Regarding claim 5, the method of claim 4, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (58:19 – 23, see solving and machine configuration file 1328).

Regarding claim 6, the method of claim 3, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (58:20 – 23, see configuration file, register file sizes and architecture specific files).

Regarding claim 7, the method of claim 1, wherein the hardware characteristics include at least one of clock speed of the processor, processor model, cache

configuration of the system, hardware operation latency times, and instruction set characteristics (58:20 – 35, see differing cycle times, for latency times).

Regarding claim 8, the method of claim 1, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (58:18 – 23, see machine configuration file, for system configuration data file).

Regarding claim 9, a computer-implemented method for switching between multiple implementations of a routine in a library of routines that are linked with an application program hosted by a computer system, comprising:

establishing a set of hardware configuration characteristics that describe the computer system (58:18 – 23, see configuration file);

establishing a symbol table, the symbol table having one or more entries that include a name of a routine, a set of hardware characteristics, and an address referencing a routine in the library (60:35 – 40, see symbol table, see fig 13, 1308, 1310);

obtaining a name of a routine having multiple implementations when the library is loaded with the application program into memory of the computer system (58:11-17);

matching the name of the routine and the set of hardware configuration characteristics that describe the computer system to an entry in the symbol table (58:11 – 17, see selecting); and

generating an address in executable code for references to the routine having multiple implementations when the library is loaded with the application program, the address referencing an implementation in the library as identified in the matching step by the entry in the symbol table (12:60 – 65).

Regarding claim 10, the method of claim 9, wherein the hardware configuration characteristics include at least one of clock speed of the processor, processor model, cache configuration of the system, hardware operation latency times, and instruction set Characteristics (58:24 – 35, for atleast one of as claimed see instruction set characteristics, see RISC AND CISC).

Regarding claim 11, the method of claim 10, wherein the resolving step further comprises obtaining the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (58:18 – 23, see configuration file).

Regarding claim 12, the method of claim 9, wherein the resolving step further comprises obtaining
the hardware configuration of the system from at least one of a system configuration data file, one or more system identification registers, and system firmware (58:18 – 23, see configuration file).

Regarding claim 13, Chan anticipates, an apparatus for switching between multiple implementations of a routine in a library of routines that are linked with an application program that is hosted by a computer system, comprising:

means for compiling a plurality of implementations of a routine into respective object code modules, the routine having an associated name and each implementation adapted to a selected hardware configuration (60:30 – 35);

means for associating the object code modules with the name of the routine and respective sets of hardware characteristics(60:35 – 40, see symbol table); and

means for resolving when the application program is loaded into memory of the computer system, a reference to the routine using the sets of hardware characteristics and a hardware configuration of the system (55:60 – 65).

Regarding claim 14, Chan anticipates a computer-implemented symbol table for referencing a library of object code modules that implement a plurality of routines, comprising:

a first set of one or more entries, each entry in the first set including a unique name of a routine and a reference to an object code module in the library (60:35-40, see symbol table, see fig 13, 1308, 1310); and

a second set of one or more entries, each entry in the second set including a shared name of a routine, a set of hardware characteristics, and a reference to an object code module in the library see fig 13, 1308, 1310,see type table).

Regarding claim 15, the symbol table of claim 14, wherein the hardware characteristics include at least one of clock speed of the processor, processor model, cache configuration of the system, hardware operation latency times (for atleast one of see, 54:60-65, see performance), instruction set characteristics, bypass characteristics, branch prediction behavior, pre-fetching capability, information describing stall conditions, branch penalties, size and associativity of processor data structures (58:18 – 23, see configuration file, and register file sizes), queue sizes for out-of-order or decoupled processors, and the number of processors in a multiprocessor system.

Response to Arguments

5. Applicant's arguments filed 1/27/2004 have been fully considered but they are not persuasive to overcome the previous rejection as will be discussed below.

Argument (1), in claim 1 and 16, Applicant argues that Chan doesn't teach " compiling a plurality of implementations of a routine into respective object code modules...associating the object code modules with the name of the routine and respective sets of hardware characteristics...".

Response (1), contrary to Applicant's argument in claim 1, Chan does disclose compiling a plurality of implementations in respective object code and associating code with hardware characteristics and hardware. See Chan 60: 13 – 17, " maps register requirements expressed in low level compiler intermediate representation 1338 (object code) into register set of the target platform..." also see 60:33 – 35, "The object code is packed into precise bit patterns expected by the underlying hardware.", Examiner believes this to be equivalent to Applicant's limitations.

Argument (2), regarding Applicant's request for clarification in claims 2 – 4. See claims as set forth above.

Argument (3), regarding Applicant's argument in claim 5, 6 & 8, Applicant argues that Chan doesn't disclose,"...resolving a reference to a routine by using a configuration data file, system identification registers, or system firmware when the program is loaded".

Response (3), Examiner believes that Prior art does disclose this feature. As set forth above in claim 5 – 8, see claims for mapping. Applicant uses the phrase "at least one of a...", in claims, as interpreted Examiner is only required to map one element claimed. For example, in claim 5 Applicant discloses, "at least one of a system configuration data file, one or more system identification registers, and system firmware", see 58:19 – 23, for solving and machine configuration file 1328. For claims 6 – 8, see claims as mapped above.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

7. Any inquires concerning this communication or earlier communications from the examiner should be directed to Chuck O. Kendall who may be reached via telephone at (703) 308-6608. The examiner can normally be reached Monday through Friday between 8:00 A.M. and 5:00 P.M. est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam *can be* reached at *(703) 305-4552.*

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is *(703) 305-3900.*

For facsimile (fax) send to central FAX number 703-872-9306 *and* 703-7467240 draft

Chuck O. Kendall

Software Engineer Patent Examiner

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PRIMARY PATENT EXAMINER